L Number	Hits	Search Text	DB	Time stamp
217	91	257/E23.034.ccls. and (@ad<19990903)	USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/11/14 21:07
218	554	257/E23.055.ccls. and (@ad<19990903)	USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/11/14 20:07
219	77	(257/E23.034.ccls. and (@ad<19990903)) not (257/E23.055.ccls. and (@ad<19990903))	USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/11/14 21:13
220	2290	polyimide with ((carrier or rigid$4) and (substrate or film or tape))	USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/11/14 20:28
221	36	(polyimide with ((carrier or rigid$4) and (substrate or film or tape))) and (257/666.ccls. and (@ad<19990903))	USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/11/14 20:15
222	1	("6199743").PN.	USPAT	2004/11/14 20:15
223	13	((polyimide and ((index or sprcket) near hole$1)) with (substrate or film or tape)) and (@ad<19990903)	USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/11/14 20:35
224	354	((polyimide and ((index or sprocket) near hole$1)) with (substrate or film or tape)) and (@ad<19990903)	USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/11/14 20:36
225	1456	(((tape or polyimide) and ((index or sprocket) near hole$1)) with (substrate or film or tape)) and (@ad<19990903)	USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/11/14 20:37
226	525	((((tape or polyimide) and ((index or sprocket) near hole$1)) with (substrate or film or tape)) and (@ad<19990903)) and ((chip or chips or die or dies) with (substrate or tape or polyimide))	USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/11/14 20:40
227	406	(((((tape or polyimide) and ((index or sprocket) near hole$1)) with (substrate or film or tape)) and (@ad<19990903)) and ((chip or chips or die or dies) with (substrate or tape or polyimide))) and (LOC or leads or wire or wires or (lead near chip))	USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/11/14 20:41
228	406	(((((tape or polyimide) and ((index or sprocket) near hole$1)) with (substrate or film or tape)) and (@ad<19990903)) and ((chip or chips or die or dies) with (substrate or tape or polyimide))) and (LOC or LUC or leads or wire or wires or (lead near chip))	USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/11/14 20:42
229	306	((((((tape or polyimide) and ((index or sprocket) near hole$1)) with (substrate or film or tape)) and (@ad<19990903)) and ((chip or chips or die or dies) with (substrate or tape or polyimide))) and (LOC or LUC or leads or wire or wires or (lead near chip))) not (257/E23.055.ccls. and (@ad<19990903))	USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/11/14 20:51
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231	4	(("5789820") or ("5945834") or ("6362637") or ("6670696")).PN.	USPAT	2004/11/14 20:55
232	2	"58074064"	JPO; DERWENT	2004/11/14 20:56
233	2	"60046059"	JPO; DERWENT	2004/11/14 20:57

234	2	"11274348"	JPO; DERWENT	2004/11/14 20:57
235	146	257/668.ccls. and (@ad<19990903) and (reinforcing or reinforce or rigid or stiffner)	USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/11/14 21:16
236	121	(257/668.ccls. and (@ad<19990903) and (reinforcing or reinforce or rigid or stiffner)) not (257/E23.055.ccls. and (@ad<19990903))	USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/11/14 21:17
237	402	257/668.ccls. and (@ad<19990903) and (carrier or reinforcing or reinforce or rigid or stiffner)	USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/11/14 21:16
238	281	(257/668.ccls. and (@ad<19990903) and (carrier or reinforcing or reinforce or rigid or stiffner)) not ((257/668.ccls. and (@ad<19990903) and (reinforcing or reinforce or rigid or stiffner)) not (257/E23.055.ccls. and (@ad<19990903)))	USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/11/14 21:17
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-	2727	((chip or chips or die or dies) with (substrate or tape)) and (LOC or (lead near chip))	USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/11/14 20:41

-	2727	(((chip or chips or die or dies) with (substrate or tape)) and (LOC or (lead near chip))) and (ad<19990903)	USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/11/13 10:56
-	1869	(((chip or chips or die or dies) with (substrate or tape)) and (LOC or (lead near chip))) and (@ad<19990903)	USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/11/13 11:00
-	1247	((((chip or chips or die or dies) with (substrate or tape)) and (LOC or (lead near chip))) and (@ad<19990903)) and (wire or wires)	USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/11/13 10:59
-	1574	polyimide with rigid$4	USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/11/13 11:04
-	86	(((chip or chips or die or dies) with (substrate or tape)) and (LOC or (lead near chip))) and (polyimide with rigid$4)	USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/11/13 11:05
-	25	((((chip or chips or die or dies) with (substrate or tape)) and (LOC or (lead near chip))) and (polyimide with rigid$4)) and (@ad<19990903)	USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/11/13 11:06
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-	78	(((chip or chips or die or dies) with (substrate or tape)) and (LOC or (lead near chip))) and (polyimide with ((carreir or rigid$4) and (substrate or film or tape)))	USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/11/13 11:05
-	19	((((chip or chips or die or dies) with (substrate or tape)) and (LOC or (lead near chip))) and (polyimide with ((carreir or rigid$4) and (substrate or film or tape)))) and (@ad<19990903)	USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/11/13 11:15
-	554	257/E23.055.ccls. and (@ad<19990903)	USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/11/14 20:04
-	1	("6199743").PN.	USPAT	2004/11/13 12:18

Amagai

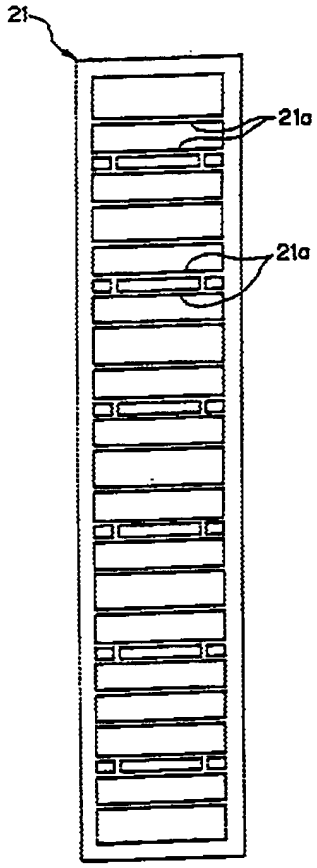

FIG. 9

Cleaved plane X pair

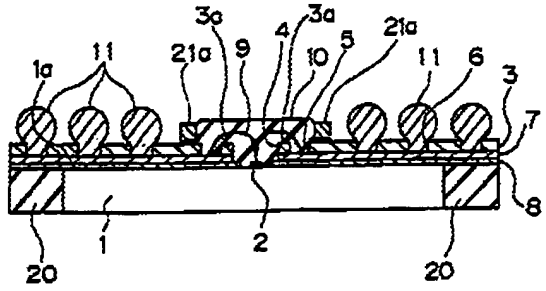

FIG. 7

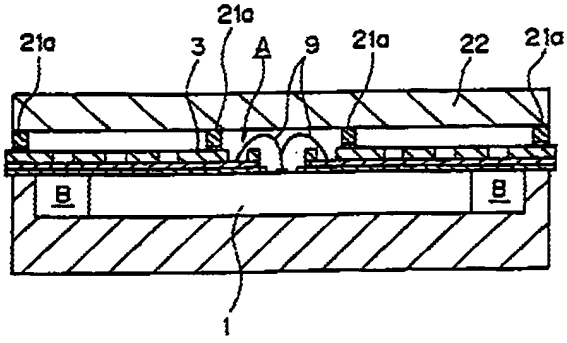

FIG. 8

(10-2)

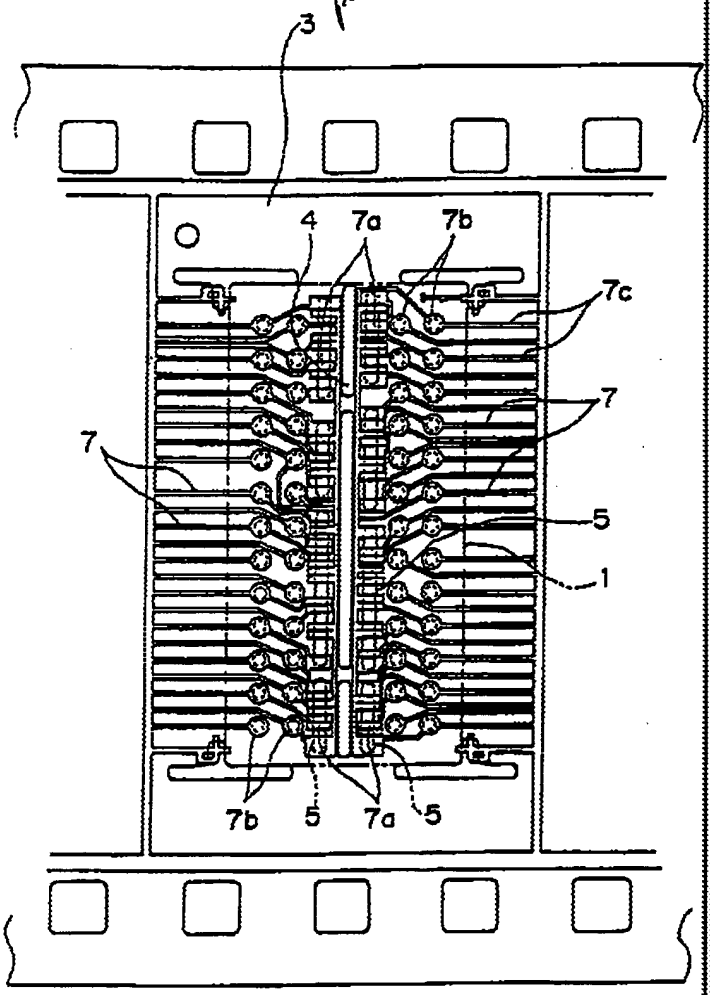

FIG. 3

the size of the chip. The aforementioned reinforcing part is preferably a resin molding.

DRAWING DESCRIPTION:

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is an oblique view of the memory device in an embodiment of this invention as seen from the assembly surface side.

FIG. 2 is a cross-sectional view of FIG. 1.

FIG. 3 is a plane view of the insulating substrate after formation of conductor leads on the insulating substrate.

FIG. 4 is a plane view of the insulating film before formation of the conductor leads on the insulating substrate.

FIG. 5 is a plane view of the principal surface side of the semiconductor device before carrying on the insulating substrate.

FIG. 6 is a diagram illustrating the step involving formation of the protective film and openings on the semiconductor chip.

FIG. 7 is a cross-sectional view of the memory device in another embodiment of this invention.

FIG. 8 is a cross-sectional view illustrating the state in which the memory device is accommodated in the molding dies.

FIG. 9 is a plane view of the lead frame.

DETAILED DESCRIPTION:

(1) REFERENCE NUMERALS AND SYMBOLS AS SHOWN IN THE DRAWINGS

(2) In the FIG. 1 represents a semiconductor chip, 1a a principal surface, 2a electrode pad, 3a a Wall, 4 an opening for electrode pad, 5 an opening for inner lead, 6 a through-hole, 7 a conductor lead, 7a an inner lead, 7b an outer lead, 7c a stub, 8 an adhesive layer, 9 a conductor wire, 10 resin, 11 a solder

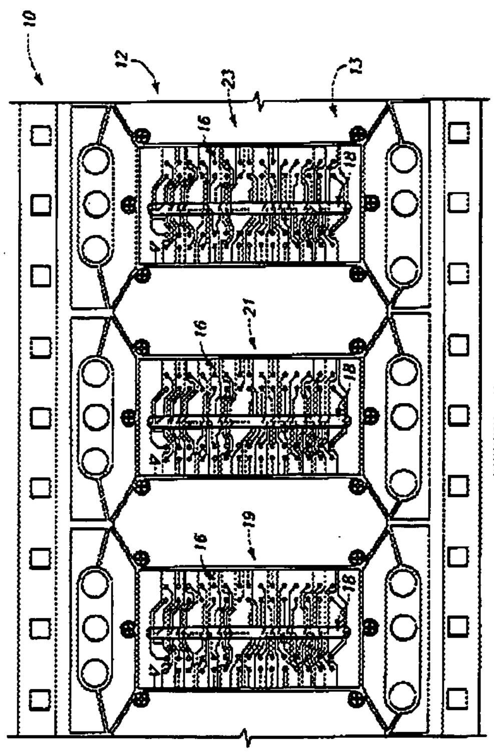

FIG. 1
PRIOR ART

(12) **United States Patent**
Bettinger et al.

(10) Patent No.: **US 6,199,743 B1**
(45) Date of Patent: **Mar. 13, 2001**

(54) APPARATUSES FOR FORMING WIRE BONDS FROM CIRCUITRY ON A SUBSTRATE TO A SEMICONDUCTOR CHIP, AND METHODS OF FORMING SEMICONDUCTOR CHIP ASSEMBLIES

(75) Inventors: Michael Bettinger, Eagle; Ronald W. Ellis; Tracy Reynolds, both of Boise, all of ID (US)

(73) Assignee: Micron Technology, Inc., Boise, ID (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 3 days.

(21) Appl. No.: 09/378,582

(22) Filed: Aug. 19, 1999

(51) Int. Cl.⁷ B23K 1/06; B21D 43/02; B21D 43/04

(52) U.S. Cl. 228/110.1; 228/123.1; 222/173.2; 228/173.1

(58) Field of Search 228/110.1, 120, 228/122.1, 123.1, 141.1, 173.1, 173.2, 122.1

(56) References Cited

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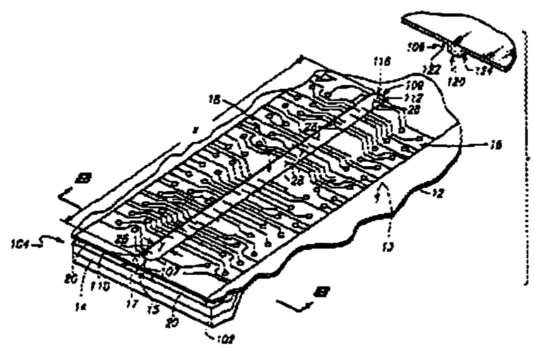
* cited by examiner

Primary Examiner—Patrick Ryan
Assistant Examiner—Jonathan Johnson
(74) *Attorney, Agent, or Firm*—Dorsey & Whitney LLP

(57) **ABSTRACT**

The invention encompasses a method of forming a semiconductor chip assembly. A substrate is provided. Such substrate has a pair of opposing surfaces and circuitry formed on one of the opposing surfaces. A semiconductor chip is joined to the substrate. The semiconductor chip has bonding regions thereon. A plurality of wires join to the circuitry and extend over the bonding regions of the semiconductor chip. The wires are pressed down to about the bonding regions of the semiconductor chip with a tool. The tool is lifted from the wires, and subsequently the wires are adhered to the bonding regions of the semiconductor chip. The invention also encompasses an apparatus for forming wire bonds from circuitry on a substrate to a semiconductor chip joined to the substrate. Such apparatus comprises a support for supporting the substrate and the semiconductor chip. The apparatus further comprises a pressing tool movably mounted relative to the substrate, and which has a deflecting surface configured to press the wires into a slit of the substrate when the pressing tool is moved toward the substrate. The deflecting surface is substantially planar, and has a sufficient length to extend within a predominant portion of the slit.

6 Claims, 6 Drawing Sheets



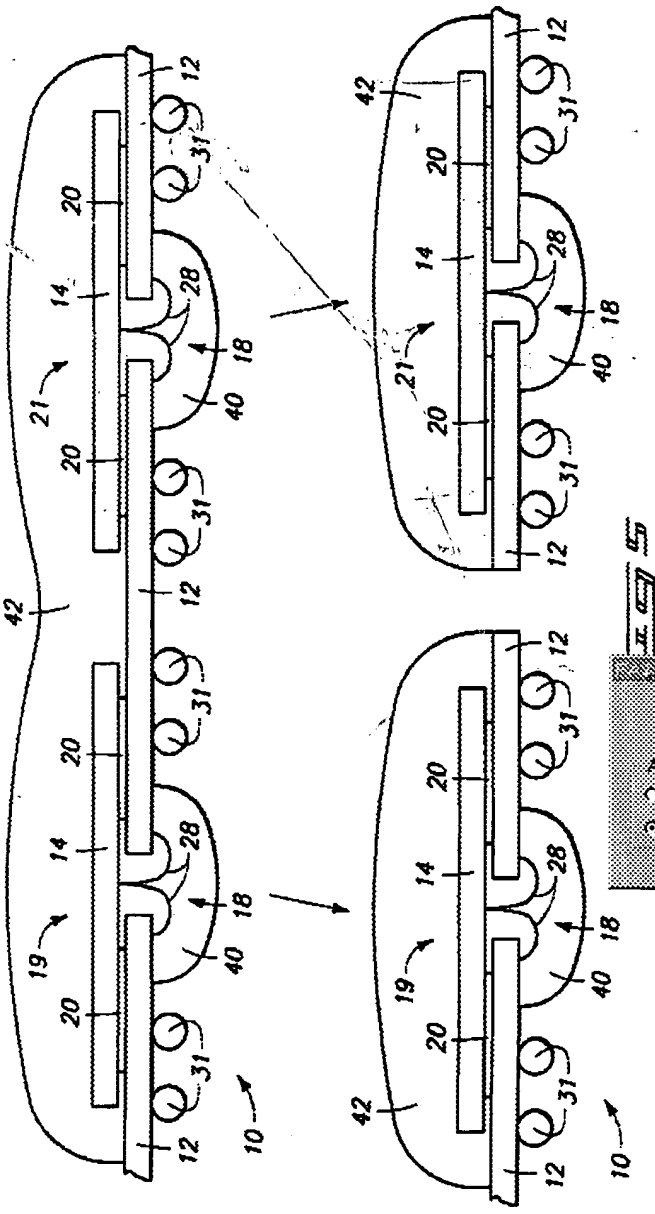


FIG. 4

US-PAT-NO: 6199743

DOCUMENT-IDENTIFIER: US 6199743 B1

TITLE: Apparatuses for forming wire bonds from circuitry on a substrate to a semiconductor chip, and methods of forming semiconductor chip assemblies

DATE-ISSUED: March 13, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Bettinger; Michael	Eagle	ID	N/A	N/A
Ellis; Ronald W.	Boise	ID	N/A	N/A
Reynolds; Tracy	Boise	ID	N/A	N/A

ASSIGNEE INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Micron Technology, Inc.	Boise	ID	N/A	N/A	02

APPL-NO: 09/ 378552

DATE FILED: August 19, 1999

Find what: 84

Area: All, Sel/Cur | Direction: Up, Down | Match word: Whole, Part | Look in: Left, Right | Grid, Documents

257/E23.024 , 257/E23.039 , 257/E23.055

FIELD-OF-SEARCH: 228/110.1; 228/120 ; 228/122.1 ; 228/123.1 ; 228/141.1 ; 228/173.1 ; 228/173.2 ; 228/121.1

REF-CITED:

U.S. PATENT DOCUMENTS

PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
3347442	October 1967	Reber	228/3
N/A	N/A		
3934783	January 1976	Larrison	228/110
N/A	N/A		
5024367	June 1991		

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File Edit View Tools Window Help

Find what: 20 | Find Next | Cancel

Area: All / Sel/Cur — Direction: Up / Down — Match word: Whole / Part / Left / Right — Look in: Grid / Documents — Match case

US005359222A

United States Patent [19]

Okutomo et al.

[11] Patent Number: 5,359,222

[45] Date of Patent: Oct. 25, 1994

[54] TCP TYPE SEMICONDUCTOR DEVICE CAPABLE OF PREVENTING CROSSTALK

[75] Inventors: Takayuki Okutomo; Morihiko Ikemizu, both of Kawasaki, Japan

[73] Assignee: Kabushiki Kaisha Toshiba, Kawasaki, Japan

[21] Appl. No.: 11,122

[22] Filed: Jan. 29, 1993

[30] Foreign Application Priority Data

Jan. 31, 1992 [JP] Japan 4-016097
Nov. 24, 1992 [JP] Japan 4-313893

[51] Int. Cl.5 .... H01L 23/48; H01L 29/44; H01L 29/52; H01L 29/60

[52] U.S. Cl. 257/659; 257/691; 257/666

[58] Field of Search 257/691, 668, 665, 668, 257/659, 660, 662; 437/217, 206, 220

[56] References Cited

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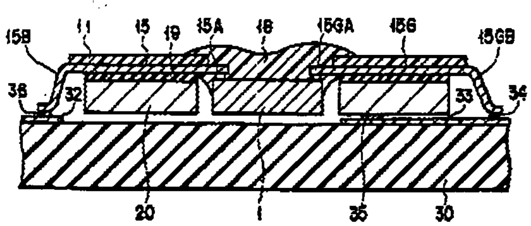
Using Advanced Pulsed Hot Bar Solder Technology for Reliable Positioning and Mounting of High Lead Count Flat Packs and Tab Devices, ITAB '90 Proceedings, pp. 230-249, (1990).

Primary Examiner—Rolf Hille
Assistant Examiner—S. V. Clark
Attorney, Agent, or Firm—Finnegan, Henderson, Farabow, Garrett & Dunner

[57] ABSTRACT

A wiring pattern having a plurality of leads is formed on the under surface of an insulating film. The inner lead portion of each of the leads is bonded to a corresponding one of bump electrodes formed on pads of a semiconductor chip and the outer lead portion thereof is connected to a corresponding lead wire formed on a printed circuit board. The outer lead portion of one of the leads which acts as a ground line is connected to a grounded lead wire which is formed on the printed circuit board. A shield plate is bonded to the under surface of the leads via insulating adhesive agent. The shield plate is electrically connected to the grounded lead wire. The semiconductor chip and the inner lead portions are hermetically sealed by use of potting resin.

9 Claims, 9 Drawing Sheets



Details | Text | Image | HTML | Full

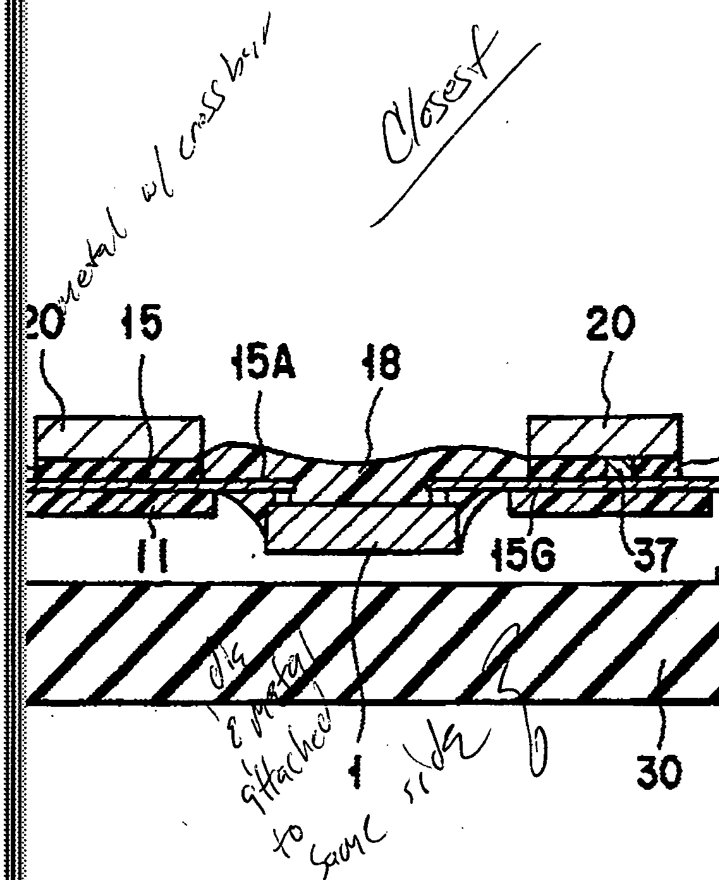


FIG. 17

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---------- KWIC ---------

Application Filing Date - AD (1):
19930129

Brief Summary Text - BSTX (6):
The carrier tape is also called a TAB (Tape Automated Bonding) tape and a wiring pattern (lead) is formed by laminating a Cu foil, for example, on an insulating film such as a polyimide film and subjecting the Cu foil to the photoetching process. A bump electrode is formed on the semiconductor chip, the wiring pattern formed on the carrier tape is bonded to the bump electrode, then potting resin is dropped on the inner lead portion of the wiring pattern and the semiconductor chip and heat treatment is effected to cure potting resin. Alternatively, the inner lead portion of the wiring pattern and the semiconductor chip are hermetically sealed by use of mold resin instead of the potting resin.

Detailed Description Text - DETX (3):
FIG. 2 shows a carrier tape used in the semiconductor device of FIG. 1 and shows a state in which the semiconductor chip 1 and the metal plate 20 are attached to the carrier tape 10 and the carrier tape 10 is not yet divided into individual semiconductor devices. A plastic film such as a polyimide or polyester film having flexibility can be used as the insulating film 11 used for a base member of the carrier tape 10. In this example, as the insulating film 11, a polyimide film which is approximately 75 to 125 .mu.m in thickness is used. The insulating film 11 is a strip-form member and feeding holes 12 used for feeding the carrier tape 10 in the lengthwise direction thereof are formed at regular intervals on both side end portions thereof. In substantially the central portion of the insulating film 11, a device hole 13 in which the semiconductor chip 1 is disposed is formed. Narrow and trapezoidal openings 14-1 to 14-4 are formed to respectively face the four sides of the device hole 13 and surround the device hole 13.

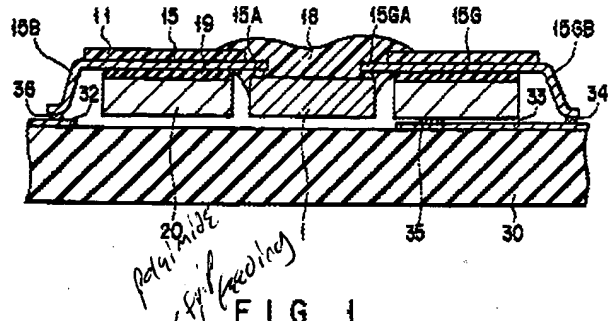

FIG. 1

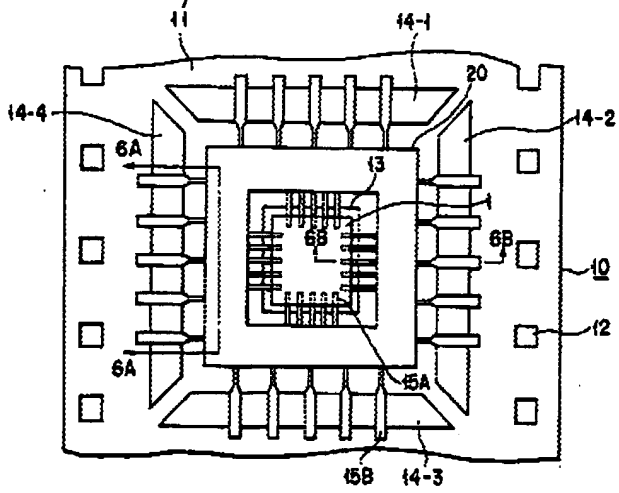

FIG. 2